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Realizability limits, distortion, and bias considerations of a bipolar active inductor

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Realizability limits, distortion, and bias considerations
of a bipolar active inductor

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by
Douglas Paul Anderson

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Graduate Faculty in Partial Fulfillment of the
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MASTER OF SCIENCE

Department: Electrical Engineering and Computer Engineering
Major: Electrical Engineering

Signatures have been redacted for privacy

Iowa State University
Ames, Iowa

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ABSTRACT

Some of the limits of realizability for a previously published active inductor circuit are explored. The circuit utilizes two bipolar junction transistors in a common collector-common emitter configuration to gyrate the base-emitter capacitance of the common emitter stage to form a synthetic inductor. This circuit has limitations, on the minimum series resistance that can be synthesized, that are inherent in the realization. The effect the bias points of the two transistors has on the quality factor Q is covered. Because the circuit utilizes active devices, there are limitations to the magnitudes of the AC voltage and current which can be applied to the inductor terminals before significant distortion occurs. Computer circuit analysis using PSpice is performed to investigate this distortion phenomenon. An additional penalty exists because the active devices consume power from DC power supplies, whereas a passive inductor does not. Bias considerations to minimize the power dissipation without compromising the circuit's performance are presented. In conclusion, it is shown that the goals of higher Q , lower distortion, and good DC power utilization are not conflicting in terms of the biasing of the transistors.

CHAPTER 1. INTRODUCTION

Statement of Problem

Active inductors present a possible alternative to using passive, lumped element inductors. When used on monolithic microwave integrated circuits (MMICs), they require less die area, have higher usable frequencies, and can potentially have higher Q's than an equivalent spiral inductor. Unfortunately, because they employ active devices, they suffer from at least two drawbacks that their passive counterparts do not. Their nonlinear effects become significant at much lower signal levels and they consume DC power.

This work will review previous work done by Campbell [1] pertaining to the theory of a particular realization of an active inductor. An expansion of the theory behind this realization will show that it has inherent limitations on the value of the series resistance, and therefore the quality factor (Q) that can be attained. Bias considerations that maximize the Q of the inductor will be explored. Then, the concepts of 1) a slightly nonlinear one-port network, 2) large-signal impedance, and 3) impedance distortion will be developed. Computer modelling in the time and frequency domain will be used to investigate the distortion of the active inductor circuit at various bias points, drive levels and frequencies. Bias considerations to minimize power

dissipation without compromising the circuit's performance will be discussed.

The conclusion of this work will show that the mutual goals of high Q , low distortion, and good utilization of DC power for this circuit are not conflicting in regards to the bias considerations of the two transistors.

Review of Past Work

The concept of replacing a wire-wound inductor with an actively synthesized inductor is not new. Various active methods for replacing large inductors at audio frequencies have been widely published. For microwave engineering, the area that currently shows the most activity is in the replacement of spiral inductors on MMICs with various active equivalents. Various gallium-arsenide field effect transistor (GaAsFET) circuits have been proposed by Hara et al. [2,3], Zhang et al. [4,5], Chien and Frey [6], Bastida et al. [7] and Morf [8].

The circuit used for this thesis is shown in figure 1.1. It was previously published by Campbell [1] and Campbell and Weber [9]. It is composed of two bipolar junction transistors (BJTs), one a common emitter and the other a common collector. They serve to gyrate the base-emitter capacitance of the common emitter stage to synthesize an inductor. This circuit also employs two series-connected parallel resistor-capacitor networks in feedback to compensate

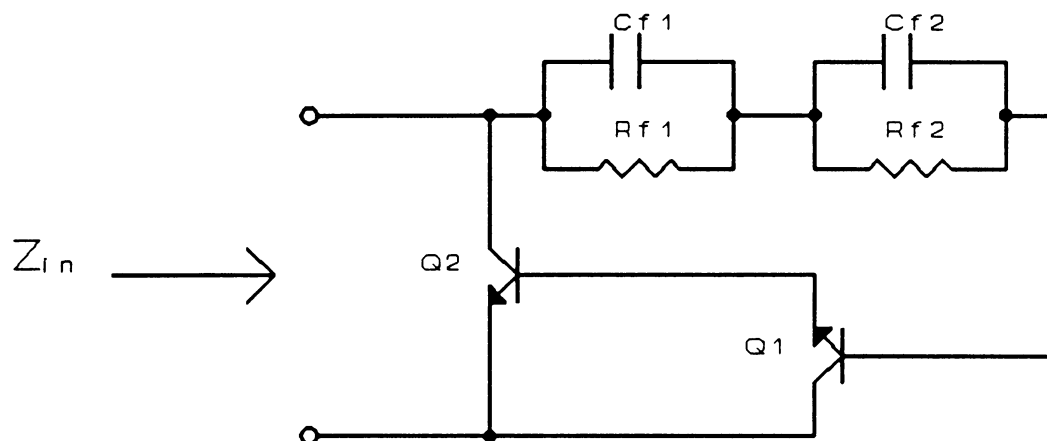


Figure 1.1 - Active inductor circuit (from Campbell [1]).

for the base-emitter poles of the two transistors. This provides a relatively constant inductance over a wide frequency range. However, it will be shown in this thesis that this realization also imposes a bound on the range of values that the equivalent series resistance may take. This, in turn, means there is a limited range to the value of the Q of the inductor.

In these previously published papers, the small-signal performance was stressed. Little, if any, investigation was made into the large signal behavior of these circuits or of the DC power requirements relative to the signal handling capability. This thesis will investigate the distortion and bias considerations of this inductor realization.

CHAPTER 2. REVIEW OF ACTIVE INDUCTOR SYNTHESIS

The realization of an active two terminal network whose input impedance is a constant inductance in series with a resistance over a very broad frequency range is covered extensively by Campbell [1]. This circuit was previously shown in figure 1.1. This chapter is a review of Campbell's work and serves as a basis for this investigation. A brief overview of the theory of this circuit follows.

When an ideal gyrator is loaded with a capacitor at its output port, the impedance seen at the input port synthesizes an inductor [10]. The voltage-controlled current sources shown in figure 2.1 realize an ideal gyrator whose z-parameter matrix is

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{g} \\ \frac{1}{g} & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (2.1)$$

The value of the inductance seen looking into port 1 is

$$L = \frac{C}{g^2} \quad (2.2)$$

The simplified single-pole, small-signal, hybrid-pi model [11] of a bipolar junction transistor contains a voltage-controlled current source. The base-emitter resistance and capacitance are included to account for the first-order

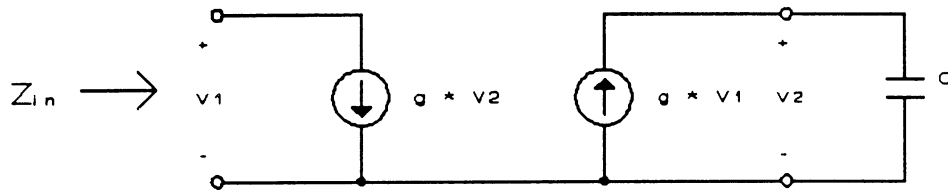


Figure 2.1 - Voltage-controlled current source gyrator realization of an ideal active inductor.

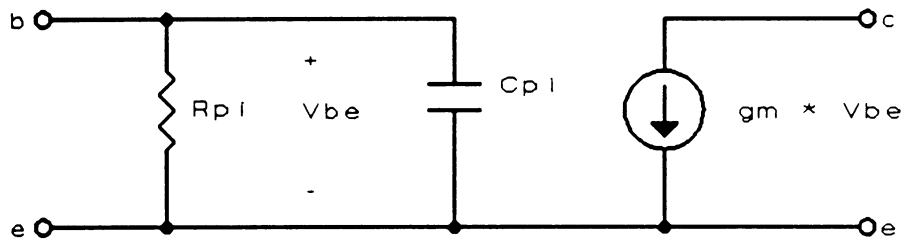


Figure 2.2 - Small-signal hybrid-pi model of a bipolar junction transistor.

effects of the frequency response of a BJT. The small-signal hybrid-pi model is shown in figure 2.2.

Two BJTs are placed in a common-emitter common-collector arrangement as shown in figure 2.3. The hybrid-pi approximations of these transistors are substituted and rearranged as shown in figure 2.4. A high impedance feedback network $Z_f(s)$ is included to provide drive to the base of Q1. By comparing this circuit to the ideal case shown in figure 2.1, it can be seen that a non-ideal active inductor is synthesized by the gyration of the base-emitter capacitance of Q2 when looking from the collector to emitter of Q2.

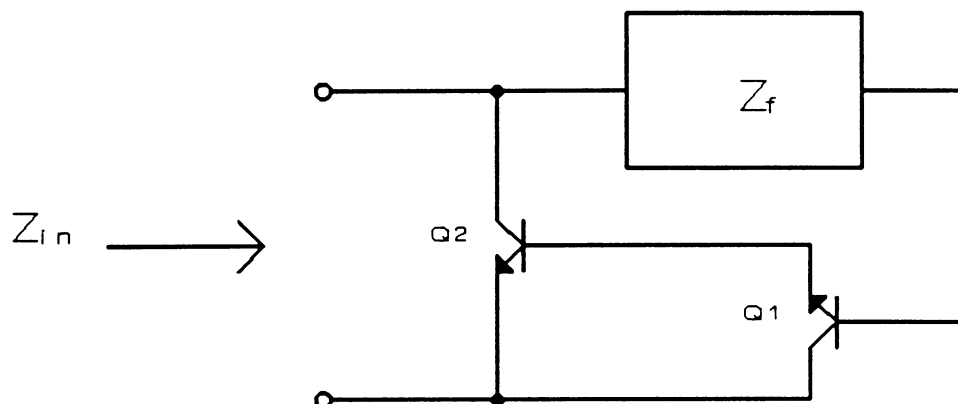


Figure 2.3 - BJT realization of active inductor.

As Campbell [1] has shown, the impedance looking into the network of figure 2.4 is given by

$$Z_{in}(s) = \frac{Z_f(s) + Z_1(s) + Z_2(s) + g_{m1}Z_1(s)Z_2(s)}{1 + g_{m2}Z_2(s)(1 + Z_1(s)g_{m1})} \quad (2.3)$$

where

$$Z_1(s) = \frac{R_{\pi 1}}{1 + sC_{\pi 1}R_{\pi 1}} \quad (2.4)$$

and

$$Z_2(s) = \frac{R_{\pi 2}}{1 + sC_{\pi 2}R_{\pi 2}} \quad (2.5)$$

To approximate the ideal gyrator more closely, $Z_f(s)$ must be a large impedance relative to $Z_1(s)$ and $Z_2(s)$ so that very little current feedback occurs. Thus, a valid approximation

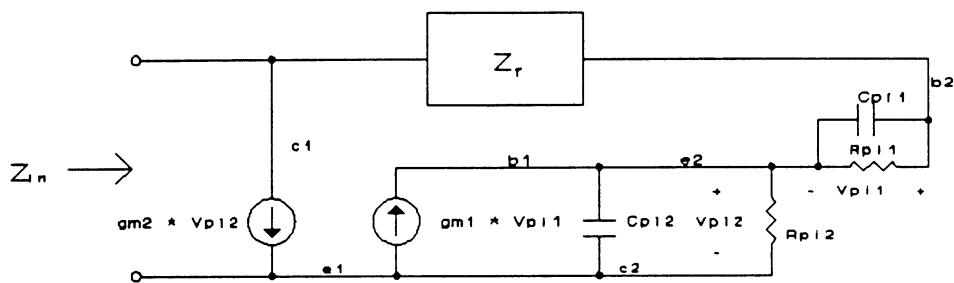


Figure 2.4 - Small-signal hybrid-pi substitution into BJT active inductor.

is

$$Z_f(s) + g_{m1}Z_1(s)Z_2(s) \gg Z_1(s) + Z_2(s) \quad (2.6)$$

and can be used to simplify the expression for the input impedance to

$$Z_{in}(s) \approx \frac{Z_f(s) + g_{m1}Z_1(s)Z_2(s)}{1 + g_{m2}Z_2(s)(1 + Z_1(s)g_{m1})} \quad (2.7)$$

The goal is to synthesize a lossless inductor. However, in the event that this circuit can not synthesize a lossless inductor, a series resistance term is included to account for the loss. It is also desirable to synthesize an inductor whose inductance is constant with frequency. Since this may also not be possible, the dependence of the inductance and resistance upon frequency is explicitly stated. Thus, $Z_{in}(s)$ above is set equal to $R_{in}(\omega) + sL_{in}(\omega)$.

Solving for $Z_f(s)$ results in

$$Z_f(s) = R_{in}(\omega) + \frac{g_{m2}L_{in}(\omega)}{C_{\pi2}} + sL_{in}(\omega) + \frac{K(s+\sigma_z)}{\left(s + \frac{1}{R_{\pi1}C_{\pi1}}\right)\left(s + \frac{1}{R_{\pi2}C_{\pi2}}\right)} \quad (2.8)$$

where

$$K = \frac{g_{m2}}{C_{\pi1}C_{\pi2}} \left(L_{in}(\omega) g_{m1} + C_{\pi1} R_{in}(\omega) - \frac{L_{in}(\omega) C_{\pi1}}{R_{\pi2} C_{\pi2}} \right) \quad (2.9)$$

$$\sigma_z = \frac{R_{in}(\omega) \left(g_{m1} + \frac{1}{R_{\pi1}} \right) - \frac{L_{in}(\omega)}{R_{\pi1} R_{\pi2} C_{\pi2}} - \frac{g_{m1}}{g_{m2}}}{L_{in}(\omega) \left(g_{m1} - \frac{C_{\pi1}}{R_{\pi2} C_{\pi2}} \right) + R_{in}(\omega) C_{\pi1}} \quad (2.10)$$

The first three terms on the right side of equation 2.8 could be realized by a resistor in series with an inductor.

However, their inclusion in the circuit would undermine the original intent of the circuit, which was to synthesize an inductor. If the impedance represented by the last term of equation 2.8 is made much larger than the first three terms, then these first three series elements may be neglected.

$$Z_f(s) \approx \frac{K(s+\sigma_z)}{\left(s + \frac{1}{R_{\pi1}C_{\pi1}}\right)\left(s + \frac{1}{R_{\pi2}C_{\pi2}}\right)} \quad (2.11)$$

In general, a real rational function can be the driving point impedance of a one port network if and only if all the poles and zeros are simple, lie on the negative real axis, and alternate with each other, the first critical frequency being a pole [10]. For the function in equation 2.11, this implies that the zero must fall between the two poles. Thus there are two possible solutions, either

$$\frac{1}{R_{\pi 1} C_{\pi 1}} > \sigma_z > \frac{1}{R_{\pi 2} C_{\pi 2}} \quad (2.12)$$

or

$$\frac{1}{R_{\pi 2} C_{\pi 2}} > \sigma_z > \frac{1}{R_{\pi 1} C_{\pi 1}} \quad (2.13)$$

This realization is in the form of two parallel RC networks connected in series as shown in figure 2.5. The values of these feedback elements are given by

$$R_{f1} = R_{\pi 1} C_{\pi 1} A \quad (2.14)$$

$$C_{f1} = \frac{1}{A} \quad (2.15)$$

$$R_{f2} = R_{\pi 2} C_{\pi 2} B \quad (2.16)$$

$$C_{f2} = \frac{1}{B} \quad (2.17)$$

with

$$A = \frac{K \left(\sigma_z - \frac{1}{R_{\kappa 1} C_{\kappa 1}} \right)}{\frac{1}{R_{\kappa 2} C_{\kappa 2}} - \frac{1}{R_{\kappa 1} C_{\kappa 1}}} \quad (2.18)$$

$$B = \frac{K \left(\sigma_z - \frac{1}{R_{\kappa 2} C_{\kappa 2}} \right)}{\frac{1}{R_{\kappa 1} C_{\kappa 1}} - \frac{1}{R_{\kappa 2} C_{\kappa 2}}} \quad (2.19)$$

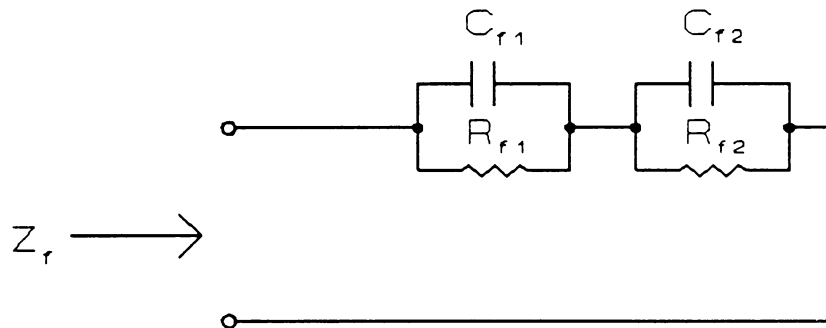


Figure 2.5 - Feedback network realization.

CHAPTER 3. REALIZABILITY LIMITS OF THE ACTIVE INDUCTOR

Region of Realizability

As stated in chapter 2, in order to realize $Z_f(s)$ as an RC network, it is necessary to have the zero of the driving point impedance function for the feedback network lie between its two poles. Depending on whether $1/R_{\pi 1}C_{\pi 1}$ is greater or less than $1/R_{\pi 2}C_{\pi 2}$, either equation 2.12 or 2.13 apply. It will be shown later that which one is greater is determined by the bias of Q1 and Q2. In either case, σ_z is bounded on one side by $1/R_{\pi 1}C_{\pi 1}$ and on the other side by $1/R_{\pi 2}C_{\pi 2}$. As shall now be shown, this implies that once the bias is set on Q1 and Q2, and therefore the values of the elements in the hybrid-pi model are determined, and once the desired value of inductance is chosen, there are limits on the range of the series resistance that can be synthesized by this circuit.

First, the limit where σ_z equals $1/R_{\pi 1}C_{\pi 1}$ shall be investigated. Setting the right side of equation 2.10 equal to $1/R_{\pi 1}C_{\pi 1}$ gives

$$\frac{1}{R_{\pi 1}C_{\pi 1}} = \frac{R_{in}(\omega) \left(g_{m1} + \frac{1}{R_{\pi 1}} \right) - \frac{L_{in}(\omega)}{R_{\pi 1}R_{\pi 2}C_{\pi 2}} - \frac{g_{m1}}{g_{m2}}}{L_{in}(\omega) \left(g_{m1} - \frac{C_{\pi 1}}{R_{\pi 2}C_{\pi 2}} \right) + R_{in}(\omega) C_{\pi 1}} \quad (3.1)$$

Multiplying the denominators of both sides across and simplifying yields

$$\begin{aligned}
L_{in}(\omega) \left(g_{m1} - \frac{C_{\pi 1}}{R_{\pi 2} C_{\pi 2}} \right) + R_{in}(\omega) C_{\pi 1} \\
= R_{in}(\omega) (g_{m1} R_{\pi 1} C_{\pi 1} + C_{\pi 1}) - L_{in}(\omega) \frac{C_{\pi 1}}{R_{\pi 2} C_{\pi 2}} - \frac{g_{m1}}{g_{m2}} R_{\pi 1} C_{\pi 1}
\end{aligned} \tag{3.2}$$

Two of the terms are present on both side of the equation.

Eliminating these gives

$$L_{in}(\omega) g_{m1} = R_{in}(\omega) g_{m1} R_{\pi 1} C_{\pi 1} - \frac{g_{m1}}{g_{m2}} R_{\pi 1} C_{\pi 1} \tag{3.3}$$

Solving this for $R_{in}(\omega)$ yields

$$R_{in(1)}(\omega) = L_{in}(\omega) \frac{1}{R_{\pi 1} C_{\pi 1}} + \frac{1}{g_{m2}} \tag{3.4}$$

where the (1) subscript denotes that this is for the case where σ_z is set equal to $1/R_{\pi 1} C_{\pi 1}$.

The limit where σ_z equals $1/R_{\pi 2} C_{\pi 2}$ is investigated in a similar manner. Setting the right side of equation 2.10 equal to $1/R_{\pi 2} C_{\pi 2}$ gives

$$\frac{1}{R_{\pi 2} C_{\pi 2}} = \frac{R_{in}(\omega) \left(g_{m1} + \frac{1}{R_{\pi 1}} \right) - \frac{L_{in}(\omega)}{R_{\pi 1} R_{\pi 2} C_{\pi 2}} - \frac{g_{m1}}{g_{m2}}}{L_{in}(\omega) \left(g_{m1} - \frac{C_{\pi 1}}{R_{\pi 2} C_{\pi 2}} \right) + R_{in}(\omega) C_{\pi 1}} \tag{3.5}$$

Cross-multiplying the denominators and simplifying yields

$$\begin{aligned}
L_{in}(\omega) \left(g_{m1} - \frac{C_{\pi 1}}{R_{\pi 2} C_{\pi 2}} \right) + R_{in}(\omega) C_{\pi 1} \\
= R_{in}(\omega) \left(g_{m1} R_{\pi 2} C_{\pi 2} + \frac{R_{\pi 2} C_{\pi 2}}{R_{\pi 1}} \right) - \frac{L_{in}(\omega)}{R_{\pi 1}} - \frac{g_{m1}}{g_{m2}} R_{\pi 2} C_{\pi 2}
\end{aligned} \tag{3.6}$$

For this case, there are no terms which cancel. Rewriting to get all terms with $L_{in}(\omega)$ on one side and all term with $R_{in}(\omega)$ on the other yields

$$\begin{aligned} L_{in}(\omega) \left(g_{m1} + \frac{1}{R_{\pi 1}} - \frac{C_{\pi 1}}{R_{\pi 2} C_{\pi 2}} \right) \\ = R_{in}(\omega) \left(g_{m1} R_{\pi 2} C_{\pi 2} + \frac{R_{\pi 2} C_{\pi 2}}{R_{\pi 1}} - C_{\pi 1} \right) - \frac{g_{m1}}{g_{m2}} R_{\pi 2} C_{\pi 2} \end{aligned} \quad (3.7)$$

Solving this for $R_{in}(\omega)$ yields

$$R_{in(2)}(\omega) = L_{in}(\omega) \frac{1}{R_{\pi 2} C_{\pi 2}} + \frac{1}{g_{m2}} \frac{1}{\left(1 + \frac{R_{\pi 2} C_{\pi 2} - R_{\pi 1} C_{\pi 1}}{g_{m1} R_{\pi 1} R_{\pi 2} C_{\pi 2}} \right)} \quad (3.8)$$

where the (2) subscript denotes that this is for the case where σ_z is set equal to $1/R_{\pi 2} C_{\pi 2}$.

Plotting the lines given by equations 3.4 and 3.8 on a graph with the vertical axis representing $R_{in}(\omega)$ and the horizontal axis representing $L_{in}(\omega)$ will show the region of possible combinations of inductance and series resistance that may be synthesized by the circuit once the bias points are established. This region of realizability is the region between these two lines.

An example of such a plot is shown in figure 3.1. The following circuit elements were used to create this plot: $g_{m1} = 0.109 \text{ } \bar{U}$, $R_{\pi 1} = 977 \text{ } \Omega$, $C_{\pi 1} = 4.11 \text{ pF}$, $g_{m2} = 0.342 \text{ } \bar{U}$, $R_{\pi 2} = 373 \text{ } \Omega$, $C_{\pi 2} = 7.63 \text{ pF}$, $R_{\pi 1} = 10.767 \text{ k}\Omega$, $C_{\pi 1} = 0.373 \text{ pF}$, $R_{\pi 2} = 9.621 \text{ k}\Omega$, and $C_{\pi 2} = 0.296 \text{ pF}$. The origin of these specific numbers will be covered later. They are the result of the Case 1 bias

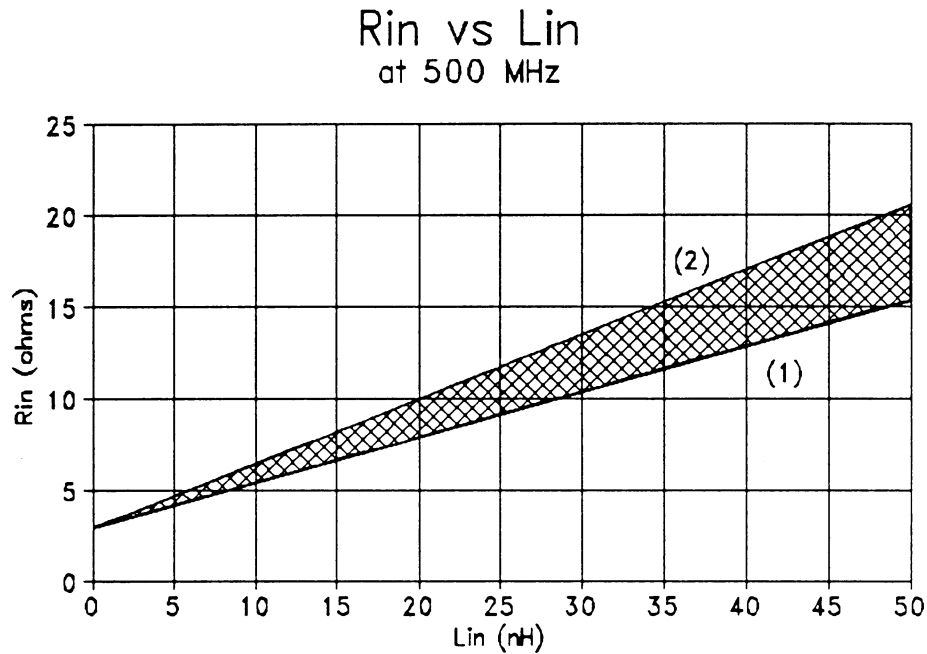


Figure 3.1 - Plot showing an example of the region of realizability of the series resistance vs. inductance for the active inductor circuit.

discussed in chapter 4. For this case, equation 3.4 gives the lower bound on $R_m(\omega)$ and equation 3.8 is the upper bound.

Another important parameter related to inductors is the quality factor Q of the inductor. Q is defined for any circuit as 2π times the ratio of the maximum instantaneous energy stored in the circuit to the energy dissipated per cycle by the circuit. Q also exhibits a dependence to frequency. For an inductor with series resistance, this simplifies to [12]

$$Q(\omega) = \frac{\omega L}{R} = \frac{\omega L_{in}(\omega)}{R_{in}(\omega)} \quad (3.9)$$

Obviously, since $R_{in}(\omega)$ for the active inductor is bounded, $Q(\omega)$ must also be bounded. Substituting equations 3.4 and 3.8 into 3.9 give the value of the two bounds for $Q(\omega)$.

$$Q_{(1)}(\omega) = \frac{\omega}{\frac{1}{R_{\pi 1} C_{\pi 1}} + \frac{1}{L_{in}(\omega) g_{m2}}} \quad (3.10)$$

$$Q_{(2)}(\omega) = \frac{\omega}{\frac{1}{R_{\pi 2} C_{\pi 2}} + \frac{1}{L_{in}(\omega) g_{m2}} \left(1 + \frac{R_{\pi 2} C_{\pi 2} - R_{\pi 1} C_{\pi 1}}{g_{m1} R_{\pi 1} R_{\pi 2} C_{\pi 2}} \right)} \quad (3.11)$$

A plot of the region of realizability of Q at 500 MHz for the example circuit elements given above is shown in figure 3.2. For this case, equation 3.10 gives the upper bound on Q and equation 3.11 is the lower bound.

Maximization of Q

It is desirable in most applications to have the Q of the inductor as high as possible. This brings forth the question as to which limit is higher, $Q_{(1)}(\omega)$ or $Q_{(2)}(\omega)$? Since higher Q implies lower series resistance, it is possible to examine equations 3.4 and 3.8 to see which one is the minimum bound.

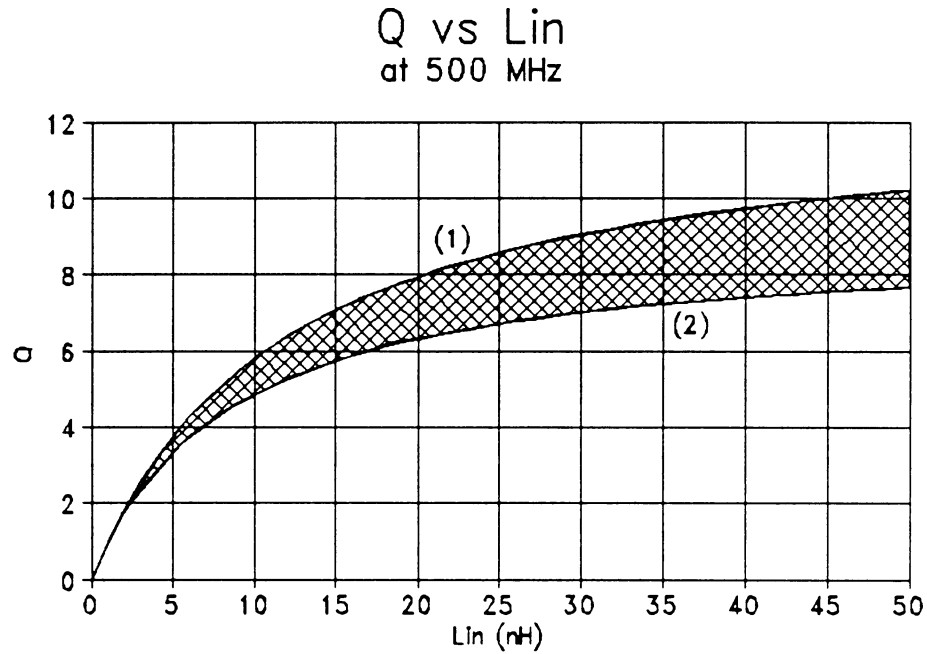


Figure 3.2 - Plot showing an example of the region of realizability of Q vs. inductance for the active inductor circuit.

The point at which the two bounds intercept the $R_{in}(\omega)$ axis can be found by setting $L_{in}(\omega) = 0$.

$$R_{in(1)}(\omega)|_{L_{in}(\omega)=0} = \frac{1}{g_{m2}} \quad (3.12)$$

$$R_{in(2)}(\omega)|_{L_{in}(\omega)=0} = \frac{1}{g_{m2}} \frac{1}{\left(1 + \frac{R_{\pi 2} C_{\pi 2} - R_{\pi 1} C_{\pi 1}}{g_{m1} R_{\pi 1} R_{\pi 2} C_{\pi 2}}\right)} \quad (3.13)$$

From equations 3.12 and 3.13, it can be seen that when $R_{r1}C_{r1}$ is greater than $R_{r2}C_{r2}$, the $R_{in(1)}(\omega)$ intercept is lower than the $R_{in(2)}(\omega)$ intercept. Equations 3.4 and 3.8 show that for this case the slope of the line for $R_{in(1)}(\omega)$ is less than the slope for $R_{in(2)}(\omega)$. Thus, the two lines never intersect and $R_{in(1)}(\omega)$ represents the minimum bound on $R_{in}(\omega)$, implying $Q_{(1)}(\omega)$ represents the maximum bound on Q . The opposite can be said for the case when $R_{r2}C_{r2}$ is greater than $R_{r1}C_{r1}$.

Since the slopes of the $R_{in(1)}$ and $R_{in(2)}$ lines are positive, the smallest value for the series resistance occurs when the minimum bound crosses the L_{in} -axis. When $R_{in(1)}$ is the minimum, equation 3.12 gives this minimum value. Obviously, it must be greater than zero, since g_{m2} is positive. When $R_{in(2)}$ is the minimum, equation 3.13 gives this minimum value. Since for this case $R_{r2}C_{r2}$ is greater than $R_{r1}C_{r1}$, then the L_{in} -axis intercept must again be greater than zero. In either case, the intercept is greater than zero. Thus, a lossless inductor cannot be realized with this circuit.

Equations 2.12 and 2.13 stated that the zero of the feedback network driving point impedance must lie between its poles. This implies that the realizability boundaries can only be approached asymptotically. Equations 2.14 through 2.19 can be used to examine what happens as these boundaries are approached. As σ_z approaches $1/R_{r1}C_{r1}$, the value of A approaches zero and the value of B approaches K . This implies

that the value of R_{f1} approaches zero while the value of R_{f2} approaches $R_{x2}C_{x2}K$, and the value of C_{f1} approaches infinity while the value of C_{f2} approaches $1/K$. Likewise, as σ_z approaches $1/R_{x2}C_{x2}$, the value of B approaches zero and the value of A approaches K , implying that the value of R_{f2} approaches zero while the value of R_{f1} approaches $R_{x1}C_{x1}K$, and the value of C_{f2} approaches infinity while the value of C_{f1} approaches $1/K$. In other words, the values of R_{f1} and R_{f2} spread farther apart in both cases, as do the values of C_{f1} and C_{f2} . Depending on the technology used to implement the active inductor, this spreading can have serious implications. For example, in an integrated circuit process, it is difficult to make resistors or capacitors on chip that differ by more than two orders of magnitude.

Implications to Transistor Biasing

For the purposes of this thesis, it will be assumed that the two transistors $Q1$ and $Q2$ are identical. This implies that the two transistors can not be biased to the same values of collector current and collector-emitter voltage, or else the base-emitter poles of both transistors would be the same, which would violate the conditions of equation 2.12 or 2.13. If it is also assumed that the collector-emitter voltage is the same for both transistors, then they must be biased to different collector currents. This leads to the question of

which transistor should have greater collector current, Q1 or Q2?

In order for the small-signal hybrid-pi model assumed by Campbell [1] to be valid, the transistors must be biased in the active region where $V_{BE} \gg kT/q$ and $V_{BC} \leq 0$, where k is Boltzmann's constant, T is absolute temperature, and q is the charge of the electron. The following is a summary of a discussion by Antognetti and Massobrio for this case [13].

The collector current can be related to the base-emitter voltage by

$$I_C = I_S e^{\frac{qV_{BE}}{kT}} \quad (3.14)$$

where I_S is a constant for a given type of transistor. Given that $V_{BE} \gg kT/q$, it takes very little variation in V_{BE} to bring about an enormous change in I_C . The pertinent elements of the hybrid-pi model are given by

$$g_m = \frac{q}{kT} I_C \quad (3.15)$$

$$R_\pi = \frac{\beta_F}{g_m} = \frac{\beta_F}{\frac{q}{kT} I_C} \quad (3.16)$$

$$C_\pi = g_m \tau_F + C_{JE}(V_{BE}) = \frac{q}{kT} \tau_F I_C + C_{JE}(V_{BE}) \quad (3.17)$$

where

$$C_{JE}(V_{BE}) = \frac{C_{JE}(0)}{F_2} \left(F_3 + \frac{m_E V_{BE}}{\phi_E} \right) \quad (3.18)$$

The parameters β_F , τ_F , $C_{JE}(0)$, F_2 , F_3 , m_E , and ϕ_E are all constants for a given transistor. Since V_{BE} does not change much, $C_{JE}(V_{BE})$ can also be treated as a constant C_{JE} .

What can be seen from these equations is that all the hybrid-pi parameters are determined by the collector current I_C . As I_C increases, g_m increases, C_r increases, and R_r decreases. Multiplying the left and right hand sides of equations 3.16 and 3.17 and treating $C_{JE}(V_{BE})$ as a constant equal to C_{JE} gives

$$R_r C_r = \beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_C} \quad (3.19)$$

So, as I_C increases, $R_r C_r$ decreases and the location of the base-emitter pole $1/R_r C_r$ increases.

The result of this discussion is that for the case where Q2 is biased with more collector current than Q1, the lower bound for $R_m(\omega)$ is given by equation 3.4 and the upper bound for $Q(\omega)$ is given by equation 3.10. When Q1 is biased with more collector current than Q2, the lower bound for $R_m(\omega)$ is given by equation 3.8 and the upper bound for $Q(\omega)$ is given by equation 3.11. But, will one of these conditions result in a higher possible $Q(\omega)$ than the other?

In the case where Q2 is biased with more collector current than Q1, the expressions for the various hybrid-pi parameters can be substituted into equation 3.4 to give

$$R_{in(1)}(\omega) = L_{in}(\omega) \frac{1}{\beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_{C2}}} + \frac{1}{\frac{q}{kT} I_{C1}} \quad (3.20)$$

This equations shows that $R_{in}(\omega)$ can be decreased by increasing I_{C2} and by decreasing I_{C1} . The only limits to minimizing $R_{in}(\omega)$ and therefore maximizing $Q(\omega)$ for this condition are the physical limits of the transistors used. I_{C2} can be increased up to its maximum allowable value. I_{C1} need only be large enough so that Q1 can be considered to be active.

For the case where Q1 has more bias that Q2, the answer is not as simple. After substituting the hybrid-pi parameter expressions into equation 3.8 and simplifying yields

$$R_{in(2)}(\omega) = \frac{L_{in}(\omega) \frac{q}{kT} I_{C2}}{\beta_F \tau_F \frac{q}{kT} I_{C2} + \beta_F C_{JE}} + \frac{\beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_{C2}}}{\beta_F \tau_F \frac{q}{kT} I_{C2} + C_{JE} \left(1 + \beta_F \frac{I_{C2}}{I_{C1}} \right)} \quad (3.21)$$

Most physical transistors have $\beta_F \gg 1$. Since it is already assumed that $I_{C1} > I_{C2}$, then $\beta_F \gg I_{C2}/I_{C1}$. This simplifies the denominator of the last term of equation 3.21 to an expression that is equal to the denominator of the other term on the right side of equation 3.21. Thus, equation 3.21 is simplified to

$$R_{in(2)}(\omega) = \frac{L_{in}(\omega) \frac{q}{kT} I_{C2} + \beta_F \tau_F + \frac{\beta_F C_{JE}}{\frac{q}{kT} I_{C2}}}{\beta_F \tau_F \frac{q}{kT} I_{C2} + \beta_F C_{JE}} \quad (3.22)$$

Now $R_{in(2)}(\omega)$ is only a function of I_{C2} and $L_{in}(\omega)$. As I_{C2} approaches zero, the rightmost terms of in the numerator and denominator of equation 3.22 become dominant and $R_{in(2)}(\omega)$ becomes inversely proportional to I_{C2} . In other words, $R_{in(2)}(\omega)$ becomes larger as I_{C2} approaches zero. For very large I_{C2} , the leftmost terms of the numerator and denominator of equation 3.22 dominate and $R_{in(2)}(\omega)$ approaches a constant value of $L_{in}(\omega) / \beta_F \tau_F$. In order to evaluate what happens between zero and infinity, the slope of the function can be evaluated. Taking the derivative of $R_{in(2)}(\omega)$ with respect to I_{C2} gives

$$\begin{aligned} & \frac{dR_{in(2)}(\omega)}{dI_{C2}} \\ & \frac{L_{in}(\omega) \beta_F C_{JE} \frac{q}{kT} - \beta_F^2 \tau_F^2 \frac{q}{kT} - 2 \frac{\beta_F^2 \tau_F C_{JE}}{I_{C2}} - \frac{\beta_F^2 C_{JE}^2}{\frac{q}{kT} I_{C2}^2}}{\left(\beta_F \tau_F \frac{q}{kT} I_{C2} + \beta_F C_{JE} \right)^2} \end{aligned} \quad (3.23)$$

Obviously, the denominator of equation 3.23 is always positive, so the only concern is the sign of the numerator. For small I_{C2} , the rightmost two terms in the numerator of equation 3.23 dominate and indicate that the function has a negative slope. For large values of I_{C2} , the leftmost two terms in the numerator dominate, but they are of opposite

sign. In order for the function to have a minimum for I_{C2} greater than zero, the slope must become positive at some point. This will only happen if

$$L_{in}(\omega) C_{JE} > \beta_F \tau_F^2 \quad (3.24)$$

In order to find the value of I_{C2} at which $R_{in(2)}(\omega)$ is a minimum, the derivative given in equation 3.23 is set equal to zero. The result can be simplified to

$$I_{C2} \Big|_{\min R_{in(2)}(\omega)} = \frac{\beta_F \tau_F C_{JE} \left(1 \pm \sqrt{\frac{L_{in}(\omega) C_{JE}}{\beta_F \tau_F^2}} \right)}{\frac{q}{kT} (L_{in}(\omega) C_{JE} - \beta_F \tau_F^2)} \quad (3.25)$$

Since I_{C2} must be greater than zero and equation 3.24 holds, then the + sign in the numerator of equation 3.25 applies.

The model parameters for an NE681 transistor are given in Appendix B. For this transistor, β_F (BF) = 185, τ_F (TF) = 1.4E-11, and C_{JE} (CJE) = 1.2E-12. Given these values, equation 3.24 implies that $L_{in}(\omega)$ must be at least 30 nH before $R_{in(2)}(\omega)$ will even have a minimum. Assuming a design value of 50 nH, the bias current I_{C2} would have to be 7.5 mA. This work is still being done under the assumption that I_{C1} is greater than I_{C2} , so for this case I_{C1} must be greater than 7.5 mA.

In the event that the desired inductance does not satisfy equation 3.24, there is no minimum in the $R_{in(2)}(\omega)$ function of equation 3.22. In this case $R_{in(2)}(\omega)$ decreases as I_{C2} increases. The best that can be attained is to set I_{C2} as close as is

comfortable to I_{C1} without exceeding I_{C1} . In this case $R_{\pi 2}C_{\pi 2}$ is nearly equal to $R_{\pi 1}C_{\pi 1}$ and equation 3.8 can be simplified to

$$R_{in(2)}(\omega) = L_{in}(\omega) \frac{1}{R_{\pi 2}C_{\pi 2}} + \frac{1}{g_{m2}} \quad (3.26)$$

Design Methodology

For this study, the following methodology was used to arrive at values for the various elements of the circuit to be simulated, which is shown in figure 3.3. All the simulations mentioned in this thesis were run on the Evaluation Version of PSpice by MicroSim Corporation, Irvine, California. Any Spice simulation software package could be used. PSpice was chosen because it includes a post-simulation graphics processing capability called Probe. PSpice is also readily available in its evaluation form, which even though limited, is sufficient for the purposes of this thesis.

First, transistors are selected and their Gummel-Poon model parameters are obtained. For this study, the model parameters were obtained from the transistor vendor.

The voltage sources V_{CE} and V_{CC} are set to the levels desired for the collector-emitter voltages of Q2 and Q1, respectively. The resistors R_{CEB} and R_{CCB} and the voltage sources V_{CEB} and V_{CCB} are then adjusted until the desired collector currents are attained in Q2 and Q1. This current

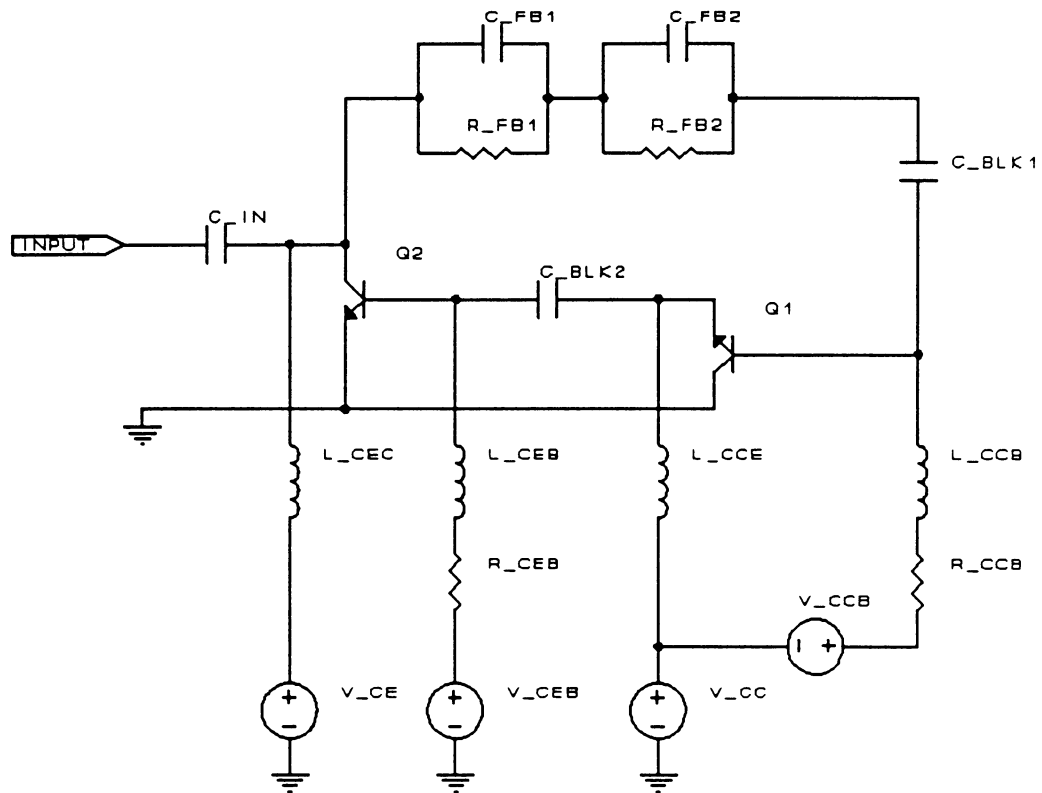


Figure 3.3 - Schematic of circuit used for simulation.

can be checked by performing a PSpice run with the .OP statement used to print a table of the operating points of Q1 and Q2. It can take several iterations of adjusting before the desired operating point is obtained.

Once the desired operating point is obtained, the table produced by the .OP statement also gives the values of g_m (GM), R_x (RPI), and C_x (CBE), which are the parameters for the hybrid- π model for the two transistors. Now that the values of these parameters are known, the equations given earlier can be used to arrive at values for the feedback elements in the

circuit that are necessary to realize the intended inductance and series resistance.

Rather than manually perform these calculations repeatedly, a program was written in Microsoft Quick-C to do this task. A brief users guide and a source listing of this program are given in Appendix A. This program asks for the pertinent hybrid-pi parameters of the two transistors and the desired value of L_m . It then responds with the minimum and maximum values of R_m that are realizable, recommends the geometric mean of these two values, and asks for the desired value. Once this information is typed in, the program responds either with the values of the four components in the feedback network or a message saying that the desired L_m and R_m cannot be realized. It then asks if the user would like to try another value of L_m and R_m for the same hybrid-pi parameters.

The values of all the components in the circuit are now defined and can be entered into the PSpice netlist for simulation.

CHAPTER 4. DISTORTION CAUSED BY THE ACTIVE INDUCTOR

Slightly Nonlinear Networks

The general theory of nonlinear networks is extremely broad. A very useful subset of this theory deals with networks that can be described by analytic transfer functions [14]. For the purposes of this thesis, such a network will be called slightly nonlinear.

Any analytic function $f(x)$ can be expanded into a Taylor series about a point $x=a$ [15], i.e.

$$f(x) = f(a) + f'(a)(x-a) + \dots + \frac{f^{(n)}(a)(x-a)^n}{n!} + \dots \quad (4.1)$$

Since slightly nonlinear networks can be characterized by analytic transfer functions, each transfer function can be expanded into a Taylor series representation about some nominal operating point. When such a network is excited by a sinusoidal forcing function such as $x=A\cos(\omega t+\varphi)$, the forced output can then be represented by the Taylor series expansion with $A\cos(\omega t+\varphi)$ substituted in for x . Expanding each term produces various integer powers of $\cos(\omega t+\varphi)$. These can then be rewritten into terms that are sinusoids at integer harmonics of the fundamental frequency ω using trigonometric identities. The result can then be written as

$$f(t) = \sum_{n=0}^{\infty} A_n \cos(n\omega t + \phi_n) \quad (4.2)$$

Thus, when a slightly nonlinear network is excited by a sinusoidal forcing function, the forced response will be a periodic function made up of components at the fundamental and harmonic frequencies of the forcing function.

Large-Signal Impedance

Impedance is, by definition, the ratio of the complex voltage across a network port relative to the complex current into that port [16]. The impedance at a particular frequency looking into a network port can be determined by applying a sinusoidal forcing function, either a voltage or current, to the port, and observing the resulting forced response, either a current or voltage. For a linear network, the response will also be a sinusoid at the same frequency as the forcing function. The impedance will then simply be the ratio of the complex voltage and the complex current. For a linear network, this ratio will be the same regardless of the amplitude of the forcing function.

When the network is slightly nonlinear, a sinusoidal forcing function will not necessarily produce a sinusoidal response. However, the response will be periodic with a fundamental component at the frequency of the sinusoidal forcing function. Since the networks that will be dealt with in this work are intended to synthesize impedance transfer functions that are positive real (i.e. their poles are in the right half plane and exclude the $j\omega$ axis), the Fourier

transform of the transfer function is equivalent to the Laplace transform of the transfer function with $s = j\omega$ [17]. Thus, the impedance can be found by taking the ratio of the Fourier transform of the steady-state forced response and the Fourier transform of the steady-state forcing function. Here the fundamental impedance $Z_{1,1}$ of a network will be defined as the ratio of the complex voltage component at the fundamental frequency to the complex current component at the fundamental frequency. Obviously, there are also cross harmonic impedances $Z_{m,n}$ formed by taking the ratio of the complex voltage component at the m th harmonic to the complex current component at the n th harmonic. When the forcing function is sinusoidal, only the $Z_{m,1}$ are obtained.

It should be noted that these impedances will in general not be independent of the amplitude of the forcing function. However, for slightly nonlinear networks the amplitude of the forcing function can usually be lowered to the point where further reduction in the amplitude will no longer produce a significant change in the value of the fundamental impedance. In other words, the magnitudes of the harmonics of the response are insignificant relative to the magnitude of the fundamental. Another way to view this is that the cross harmonic impedances become insignificant relative to the fundamental impedance. Below this amplitude, the response of the network can be considered linear and the impedance is a

small-signal impedance made up of only the fundamental impedance. Above this amplitude, the network must be considered nonlinear and the large-signal impedance is a matrix made up of the fundamental impedance and the cross harmonic impedances. Of course, this boundary between small-signal and large-signal behavior is not a well defined one and its location must be made on a case by case basis.

Impedance Distortion

If a network can be characterized by a linear transfer function, then the forced response will be a scaled replica of the forcing function. A network that is characterized by a nonlinear transfer function does not necessarily produce a forced response that is a scaled replica of the forcing function. In other words, the forced response is a distorted version of the forcing function.

There are several ways to quantify distortion, such as harmonic distortion and intermodulation distortion. For a network that is driven by a single sinusoidal forcing function, harmonic distortion is the method that is most sensible. When a slightly nonlinear network is driven by a sinusoidal forcing function, the forced response will be a periodic waveform made up of frequency components at the fundamental and harmonics of the frequency of the forcing function. Second harmonic distortion is the ratio of the magnitude of the second harmonic of the forced response to the

magnitude of the fundamental component of the forced response. Nth harmonic distortion is the ratio of the magnitude of the Nth harmonic to the magnitude of the fundamental. Total harmonic distortion (THD) is the ratio of the square root of the sum of the squares of magnitudes of all the harmonics to the magnitude of the fundamental [18], and is usually expressed in percent, i.e.

$$\%THD = \frac{\sqrt{\sum_{n=2}^{\infty} A_n^2}}{A_1} \times 100 \quad (4.3)$$

where A_n is the magnitude of the nth harmonic.

For example, if a sinusoidal current forcing function is applied to a nonlinear one-port network and the resulting voltage forced response across the port is a nonsinusoidal periodic function, then distortion has occurred. This also could be viewed as a distortion of the impedance looking into the one-port, because in addition to the lone fundamental impedance, there are now significant cross harmonic impedances. This could then be quantified in terms of harmonic distortion and total harmonic distortion.

Distortion Mechanisms of the Active Inductor

An ideal lossless, linear inductor obeys the following relationship between the voltage across it and the current through it:

$$v(t) = L \frac{di(t)}{dt} \quad (4.4)$$

where L is by definition the inductance of the inductor. When a sinusoidal current is forced through the inductor, a sinusoidal voltage is generated across the inductor that leads the current by 90° of phase. Put in phasor notation:

$$\mathbf{V} = j\omega L \mathbf{I} \quad (4.5)$$

Ideal inductors do not dissipate power. Physical inductors, however, are always lossy. This loss can be modelled as a resistance in series with the inductance. For a lossy linear inductor, the phasor relationship is then

$$\mathbf{V} = (R + j\omega L) \mathbf{I} \quad (4.6)$$

As long as the forcing function applied to the active inductor circuit presented earlier can be considered small-signal, it too will exhibit the relationship between the voltage and current that characterizes an inductor. However, as the forcing function is increased in amplitude, at some point the forced response will contain significant harmonic content.

There are several mechanisms that can cause the active inductor circuit to become nonlinear. From the theory presented earlier, the value of the inductance is determined

by the value of the feedback elements and the hybrid-pi model components. It will be assumed that the feedback elements are linear. When a transistor is driven with a large signal, the constant operating point assumption is no longer valid, i.e. the operating point varies as the drive signal swings from positive to negative peaks in a sinusoidal fashion. Thus, the hybrid-pi model components are not constant, but time varying, resulting in a distortion of the forced response.

A more pronounced distortion mechanism is caused by current limiting. The distortion should rapidly increase when the peak amplitude of the AC current through either transistor exceeds its DC bias current. Since Q1 is driving Q2, the magnitude of the AC current in Q1 is much less than in Q2, so Q2 will be the first transistor to go into current limiting. At the moment the current source driving the circuit tries to sink an amount of current equal to the bias current of Q2, the circuit can no longer provide current to Q2 and the transistor will cut off. This will result in a distortion of the voltage across the transistor. The exact shaping of the voltage while Q2 is cut off depends upon the impedance of the circuit that remains with Q2 removed. Since the voltage will be affected only during the negative peak and remain sinusoidal during the positive peak, the harmonic content can be expected to be primarily even ordered.

Another potential limiting mechanism is when the impedance of the inductor is so high that the resulting voltage waveform

pushes Q2 into saturation. This mechanism will again affect only the negative half cycle of the voltage and result in primarily even ordered harmonics.

Distortion Simulation Results

For this study, it will be assumed that the Gummel-Poon model as implemented in PSpice [19] accurately predicts the behavior of a bipolar junction transistor. Accurate modelling of the performance of bipolar junction transistors is an endeavor that has a history as old as the BJT itself. The Gummel-Poon model attempts to address more aspects of the behavior of a BJT than any other commonly available model. An extensive discussion of bipolar transistor modelling can be found in Getreu [20].

The transistor used for this work will be the NE681 from NEC for the sole reason that the vendor provides values for the various parameters of the Gummel-Poon model. The vendor-supplied parameters are presented in Appendix B.

Two active inductor circuits were developed and studied by means of simulations on PSpice. The first, which will be referred to as Case 1, has the bias for Q1 set at 8 V and 3 mA and Q2 at 8 V and 10 mA. Choosing an inductance of 5 nH forces R_m to lie between 4.169 Ω and 4.692 Ω . A value of 4.4 Ω was chosen. Case 2 has a Q1 bias of 8 V at 3 mA and Q2 at 8 V and 50 mA. An inductance of 5 nH forces a range of 1.975 Ω

to 2.584Ω for R_m . It was chosen to be 2.25Ω . The small-signal hybrid- π model parameters for the transistors under these biases, as well as the designed values of inductance and resistance and the values of the feedback elements to achieve the design goals are summarized in Table 4.1. The PSpice netlists for these circuits can be found in Appendices C and D, respectively.

Table 4.1 - Summary of simulated circuit parameters.

Parameter	Case 1 Bias	Case 2 Bias
g_{m1}	0.109 \bar{U}	0.109 \bar{U}
g_{m2}	0.342 \bar{U}	1.37 \bar{U}
R_{r1}	977 Ω	977 Ω
R_{r2}	373 Ω	69.1 Ω
C_{r1}	4.11 pF	4.11 pF
C_{r2}	7.63 pF	39.1 pF
L_{in}	5.00 nH	5.00 nH
R_{in}	4.4 Ω	2.25 Ω
R_{f1}	10767 Ω	8471 Ω
C_{f1}	0.373 pF	0.474 pF
R_{f2}	9621 Ω	6891 Ω
C_{f2}	0.296 pF	0.392 pF

Results of small-signal (AC) SPICE simulations of Case 1 and Case 2 are shown in figures 4.1 and 4.2 respectively. They show that the inductance and resistance is relatively flat from 100 MHz to 1 GHz. The inductance simulated is

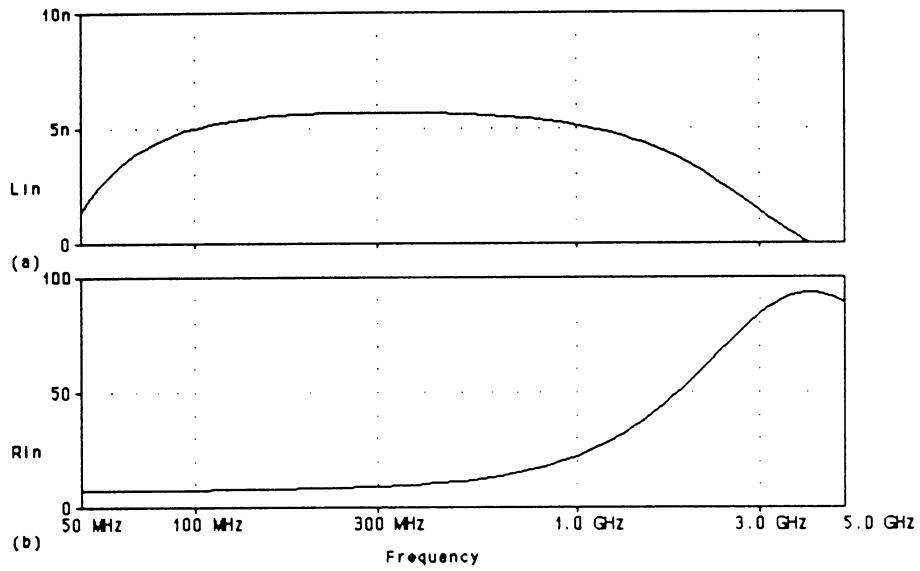


Figure 4.1 - Small-signal simulation results showing (a) inductance and (b) resistance of Case 1 circuit.

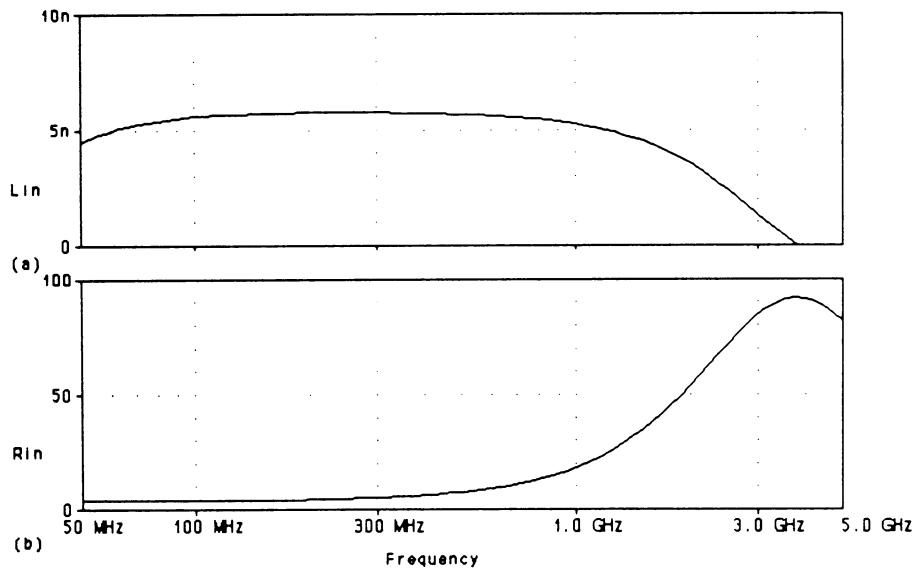


Figure 4.2 - Small-signal simulation results showing (a) inductance and (b) resistance of Case 2 circuit.

within 5% of the design value across this frequency band in both cases. The series resistance, however, is about twice as much as the design value in both cases. The rolloff at the low frequency is due to the coupling capacitors used. If larger value capacitors are used, the flatness of the inductance will extend lower in frequency. The high frequency rolloff is due to the circuit itself. As the frequency increases, the simple three element hybrid-pi model loses validity and thus the theory used to develop the circuit is no longer applicable. This phenomenon was covered by Campbell [1].

The large-signal behavior of the active inductor circuit was studied in the time domain by using the transient analysis feature of PSpice. The .FOUR statement will produce a table of the magnitude and phase of the fundamental through ninth harmonic of any node voltage or branch current desired, as well as a value for the total harmonic distortion limited to the first nine harmonics. Care was taken to insure that all the transient responses of the circuit had been sufficiently damped out before the Fourier transform was taken by extending the simulation time out as far as needed. Thus, the Fourier transform can be considered a transform of the steady-state response of the circuit.

A check can be made to verify that the transient analysis provides results for low-level signals which compare favorably with the results of the AC analysis. The magnitude and phase

of the voltage across the circuit at the fundamental frequency can be read from the Fourier component table printed by the transient analysis. This is then divided by the magnitude of the drive current, resulting in the impedance looking into the circuit. The inductance and resistance can then be computed. Table 4.2 provides a summary of inductance and resistance results from both the AC and transient analyses at several frequencies. The results from both methods are generally in good agreement, within 10%. The lack of agreement gets worse as the frequency gets lower. This may be due to the fact that the vendor supplied model for the transistor is tailored for higher frequency validity, as noted in Appendix B.

In the theory developed earlier, it was assumed that the impedance of the feedback network was much larger than the impedance looking into the collector of Q2. This would imply that the current into the active inductor flows primarily into Q2. Figure 4.3 shows the results of a simulation that was performed to observe the time-domain currents in Q1 and Q2 to verify this assumption.

Since the AC current through Q1 is much smaller than for Q2, the bias current through Q1 does not have to be as large as Q2 to avoid distortion. However, it cannot be made arbitrarily small. Q1 must be able to provide sufficient drive to Q2. Thus, a safe limit for the bias current of Q1 would be not less than a factor of one over the AC beta of Q2 less than the bias current of Q2. This should provide

Table 4.2 - AC and transient analysis results comparison.

Frequency	L_{in}	R_{in}	L_{in}	R_{in}
	Case 1 AC		Case 1 Transient	
100 MHz	5.01 nH	7.72 Ω	6.76 nH	8.94 Ω
200 MHz	5.62 nH	8.37 Ω	5.91 nH	9.93 Ω
500 MHz	5.61 nH	11.6 Ω	5.70 nH	13.5 Ω
1000 MHz	5.11 nH	22.5 Ω	5.06 nH	23.9 Ω
	Case 2 AC		Case 2 Transient	
100 MHz	5.58 nH	3.92 Ω	6.56 nH	4.09 Ω
200 MHz	5.75 nH	4.43 Ω	6.06 nH	4.92 Ω
500 MHz	5.67 nH	7.55 Ω	5.64 nH	9.22 Ω
1000 MHz	5.23 nH	18.4 Ω	5.23 nH	18.6 Ω

sufficient drive to Q2 without Q1 itself contributing to the distortion.

Figure 4.4 shows, for Case 1, the voltage across the inductor for AC current drives of 2, 3, 5, 7, and 10 mA peak. The voltage maintains a relatively sinusoidal shape up to the point where the peak amplitude of the current drive equals the bias current through Q2. When the peak current drive is equal to the Q2 bias current, Q2 will become cut off during the negative peak of the current swing, because the circuit is being forced to source more current than the Q2 bias, leaving none to flow through Q2. The voltage waveform shows an obvious departure from an ideal sinusoid at this drive level. Further increases in drive level will only increase this departure from a sinusoidal response.

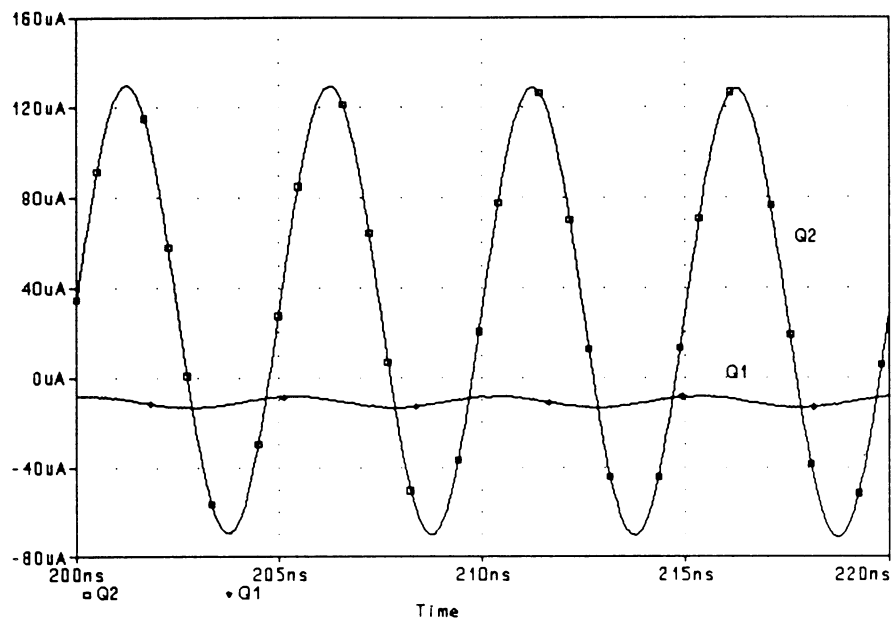


Figure 4.3 - Collector currents through Q1 and Q2. Q1 is DC offset by 3 mA and Q2 by 10 mA in order to get both on the same plot.

A plot of the amplitudes of the second through seventh harmonics, normalized to the amplitude of the fundamental, of the active inductor voltage at various drive levels for Case 1 is shown in figure 4.5. As expected, the second harmonic rises sharply once the peak current reaches the 10 mA (20 dBmA) bias current of Q2. A plot of %THD is shown in figure 4.6. The %THD is primarily determined by the amplitude of the second harmonic.

As can be seen from figures 4.7 and 4.8, the distortion stays relatively flat for low levels of drive. As the peak drive level increases to about half the value of the bias current through Q2, the distortion begins to rise into the 7

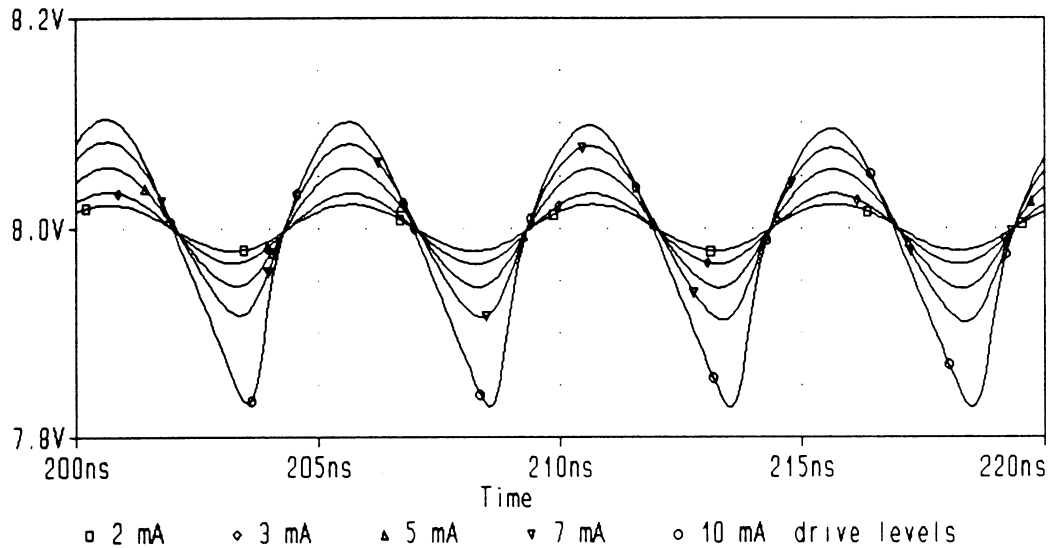


Figure 4.4 - Voltage across the inductor for current drives equal to 2, 3, 5, 7, and 10 mA peak.

to 10 percent range. At peak levels equal to the Q2 bias current, the distortion is now in the 15 to 25 percent range.

Figures 4.1 and 4.2 show that the resistance and inductance remain relatively constant from 100 MHz to 1 GHz. As the frequency of the drive current is increased, there will then be a greater voltage across the circuit, since the impedance of an inductor increases with frequency. As the voltage across the circuit increases, the assumption of small signal operation of the transistors becomes less valid. It is reasonable, then, to expect the distortion to become worse as the frequency of operation increases when the current drive

level is held constant. Figures 4.7 and 4.8 show that the distortion becomes worse at higher frequencies.

Another feature of figures 4.5, 4.6, 4.7, and 4.8 which is worth noting is the apparent increase in distortion at the lower drive levels. This was found to be due to the tolerances of the computations being performed by PSpice. At the lower drive levels, these tolerances become significant relative to the magnitude of the small AC waveforms. The relative tolerance of the computations can be adjusted by changing the RELTOL parameter within PSpice. It defaults to a value of 0.001. It was found that setting RELTOL to a value of 0.0001 will eliminate the apparent distortion at the lower drive levels.

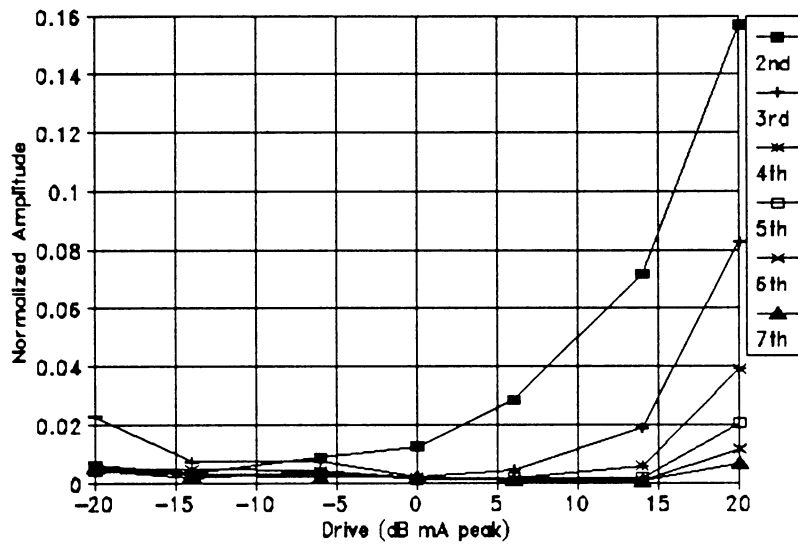


Figure 4.5 - Harmonic content at various drive levels (normalized to the amplitude of the fundamental).

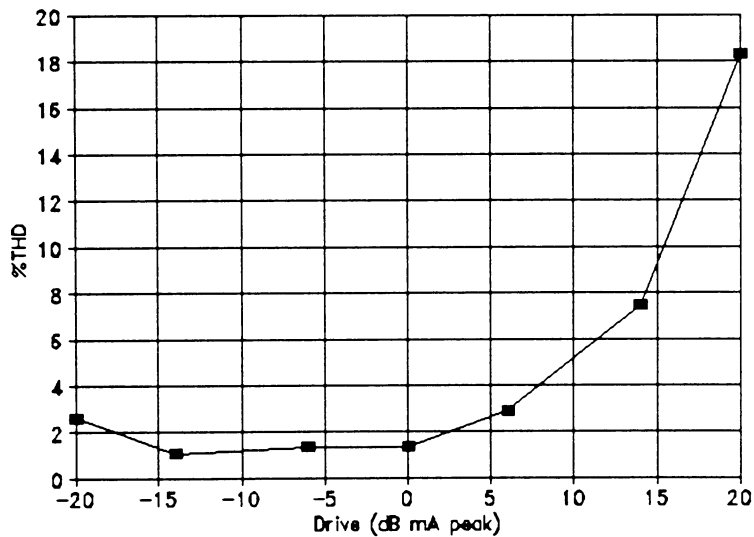


Figure 4.6 - Total harmonic distortion at various drive levels.

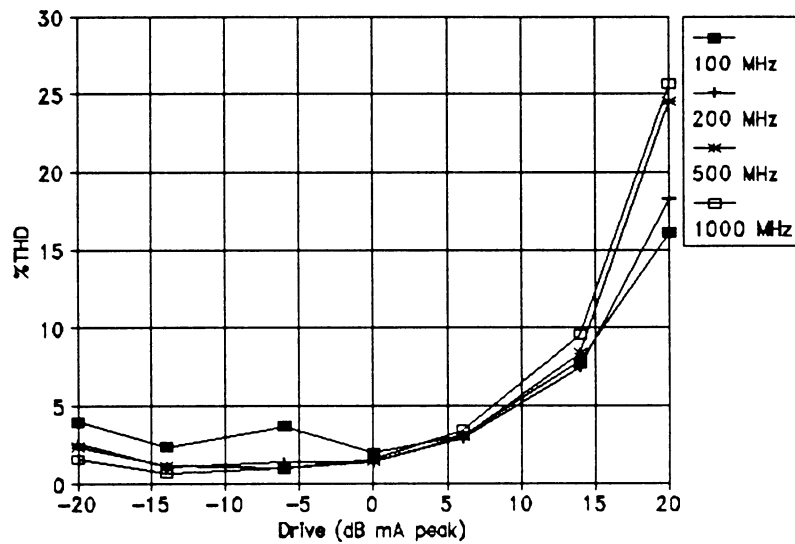


Figure 4.7 - Total harmonic distortion vs drive level at various frequencies for Case 1.

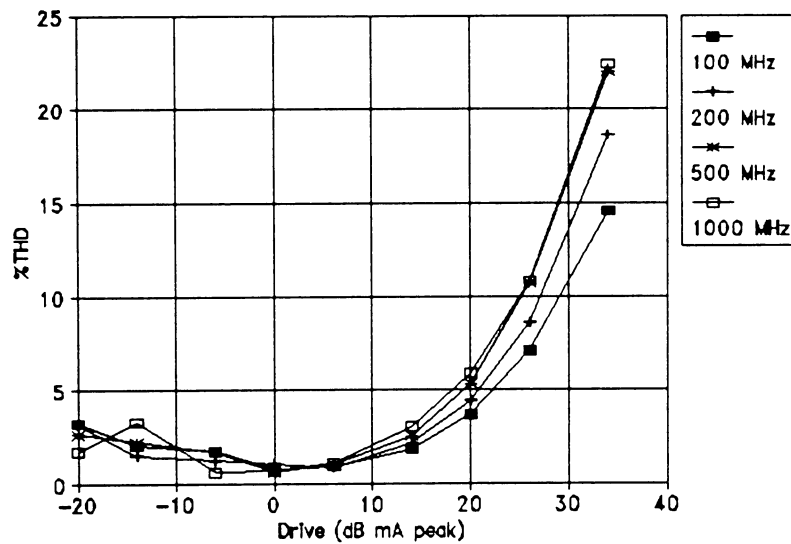


Figure 4.8 - Total harmonic distortion vs drive level at various frequencies for Case 2.

CHAPTER 5. BIAS CONSIDERATIONS FOR IMPROVED POWER UTILIZATION

Passive inductors are usually limited in their signal handling capability only by the physical constraints of the materials used in their fabrication. The AC voltage across the inductor is usually limited by the breakdown voltage of some type of insulating material used to encase the coil, including air. The current handling capability is limited by the current capacity of the conductor used for the coil or the saturation of the core. However, for an active inductor, the signal handling capability will most likely be limited by the electrical configuration of the circuit used to synthesize the inductor. As was discussed in the previous chapter, significant distortion occurs when the active inductor is driven too hard.

The passive inductor provides this signal handling capability at no cost in terms of DC power dissipation. The active inductor, however, requires DC power to bias up the active elements within the circuit.

The bias current of Q2 is the important factor in determining the maximum drive level for a given amount of distortion. Data from the simulations performed in the previous chapter are presented in figure 5.1. This figure shows that, at a fixed frequency and given distortion level, the drive level is approximately linearly related to the Q2 bias current, when voltage limiting does not occur.

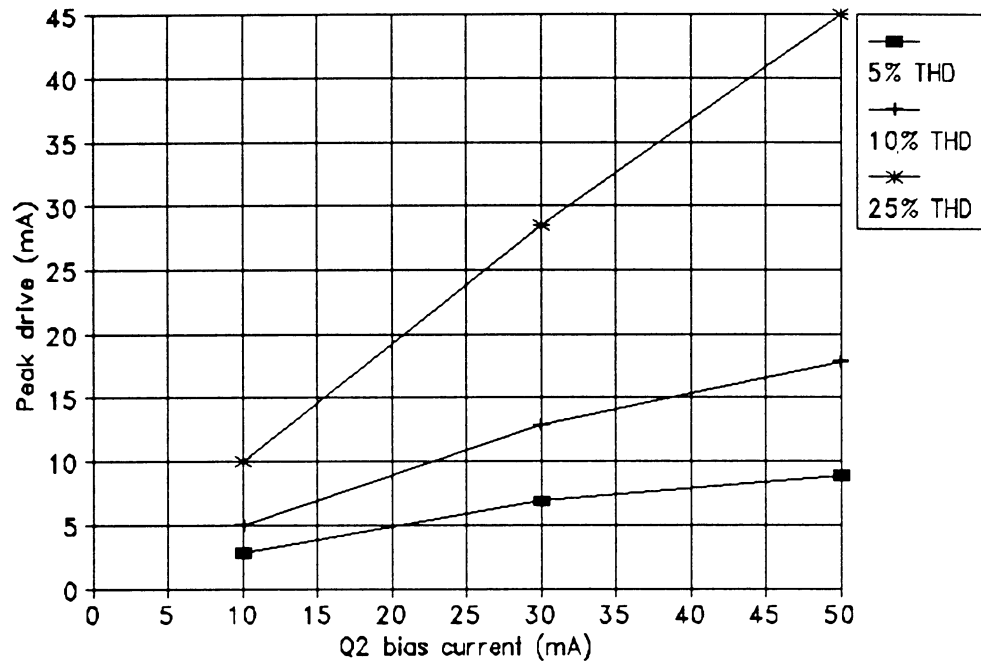


Figure 5.1 - Peak current drive vs. Q2 bias current for fixed levels of distortion at 500 MHz.

The bias current of Q1 is not nearly as important and can be set small enough compared to Q2 that it can be ignored. If an active inductor is being used in an application that demands distortion of less than 25%, then the minimum bias of Q2 must be equal to the maximum peak current level that the driving source will force through the inductor.

$$I_{pk-ac} \leq I_{dc} \quad (5.1)$$

The voltage supplied to the collector of Q2 also enters directly into the power utilization trade-off. For best

utilization, this voltage should come directly from the DC supply through a choke, otherwise additional DC power will be dissipated in a collector resistor. The collector-emitter voltage of Q2 should be kept as small as possible. However, there will once again be distortion if the negative voltage swing exceeds the collector voltage of Q2 minus the collector-emitter saturation voltage, $V_{ce(sat)}$.

$$V_{pk-ac} \leq V_{dc} - V_{ce(sat)} \quad (5.2)$$

CHAPTER 6. CONCLUSIONS

Summary

The previously published theory underlying the bipolar active inductor circuit used for this study was reviewed. The region of realizable series resistance that is possible once a value for the inductance is selected was explored. Bias considerations to maximize the quality factor of the inductor were investigated. The bias condition where the collector current of Q2 is made as large as possible and for Q1 is made as small as possible results in the greatest limiting value for Q. It was also shown that this circuit cannot realize a lossless inductor.

The concept of a slightly nonlinear network was defined, as was large-signal impedance and impedance distortion. The possible distortion mechanisms of the active inductor were discussed. The level at which distortion occurs is primarily determined by the bias on Q2. Simulations using PSpice were performed using AC, transient, and Fourier analysis to demonstrate the nonlinear performance of the active inductor as it was driven into current limiting. The results showed that at low drive levels, the small-signal and large-signal impedances were in good agreement. The results also showed that at peak current drive levels equal to the bias current of Q2, the distortion rises into the range of 16 to 25 %. The

distortion at this point is primarily contained in the second harmonic.

In order to avoid significant distortion, the bias current on Q2 must be set equal to or greater than the peak value of the AC current drive. It was shown, however, that the power dissipation of the circuit can be reduced by reducing the bias on Q1 without compromising the performance of the circuit.

Thus, the bias considerations that serve to increase Q , reduce distortion, and increase the utilization of DC power are not conflicting.

Future Work

There are several areas of continued study that are implied by this work.

The case where σ_z is set equal to $1/R_x C_x$ may bear an alternative realization for the active inductor. Also, the case where $R_{x1} C_{x1}$ is greatly different than $R_{x2} C_{x2}$ should be looked in to, as this would open up the region of realizability and give the circuit designer greater freedom.

A study of what happens if it is not assumed that the two transistors are identical, such as two transistors on a MMIC that have different base areas, would be interesting. What would be the implications to Q maximization and biasing? Which transistor should be bigger?

Applying local feedback around the two transistors would extend their bandwidth of their response at the expense of lowering their gain. Would this be of any benefit in terms of realizing an active inductor?

It would be good to verify the results of this work experimentally by building several of the circuits shown and measuring distortion at various drive levels and frequencies.

Another area is to attempt to use the models for higher bias current transistors to design an inductor that could be driven into voltage limiting and study the distortion characteristics of this mechanism alone and of simultaneous current and voltage limiting.

This study also should be repeated using models of MMIC-based transistors such as silicon bipolar and GaAs heterojunction bipolar processes. A study of the realizability limits, distortion and power utilization of the various FET active inductor circuits that have been proposed in the literature would be advised.

Another area that needs to be investigated is the noise characteristics of active inductor circuits. Since they are active, their noise will most likely be greater than that of a passive inductor.

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APPENDIX A: ACTIVE INDUCTOR DESIGN PROGRAM

A program was written in C to aid in the design of the active inductor circuit discussed in this thesis. Once this program is entered and compiled properly, it is quite simple to run. Simply type "ind" to run the program. The user will then be prompted one at a time for the following parameters of the two bipolar transistors used in the circuit: g_{m1} , g_{m2} , $R_{\pi1}$, $R_{\pi2}$, $C_{\pi1}$, and $C_{\pi2}$. The user will then be prompted to enter the desired value for the inductance of the circuit, L_m . The program will then compute the limits on R_m to make the circuit realizable. It will suggest the geometric mean value of these two limits, and then prompt the user to enter the desired value of R_m .

Upon completing this entry, the program will compute the values of the various feedback circuit elements. If data is entered that renders the circuit unrealizable, a message to this effect will be output. Otherwise, a table of all the circuit element values, both entered and computed, will be output to the screen.

The user will then be asked if another try for different values of L_m and R_m would like to be made. An answer of "N" will stop execution of the program. An answer of "Y" will again prompt the user for a desired value of L_m , show limits

and suggest a value for R_{in} , and ask for the desired value of R_{in} . The computations will again be performed and circuit elements displayed with the transistor hybrid-pi parameters left unchanged. This loop can be repeated as necessary.

No attempt has been made to check entered data for reasonableness or errors. Therefore, the burden is upon the user to enter good data.

A sample run follows. The user inputs are denoted by a >.

```
>ind
Type in value of gm1
>.109
Type in value of gm2
>.342
Type in value of Rpi1
>977
Type in value of Rpi2
>373
Type in value of Cpi1
>4.11e-12
Type in value of Cpi2
>7.63e-12
Type in desired value of Lin
>5e-9
```

Rin must lie between 4.16992e+000 and 4.6922e+000 ohms,
 suggest 4.4229e+000

Type in desired value of Rin

4.4

```
gm1 = 1.000e-001      gm2 = 3.42e-001
Rpi1 = 9.7700e+002   Rpi2 = 3.7300e+002

Cpi1 = 4.1100e-012   Cpi2 = 7.6300e-012
Lin = 5.0000e-009    Rin = 4.4000e+000

Rf1 = 1.0767e+004    Cf1 = 3.7293e-013
Rf2 = 9.6214e+003    Cf2 = 2.9580e-013
```

Want to try another value of Lin and Rin ?

>N

The program listing follows:

```
/* IND.C: Asks for simple hybrid PI parameters of two transistors, */
/* asks for Lin desired,
*/
/* then computes minimum and maximum value of Rin that is obtainable,
*/
/* asks for Rin desired and then calculates value of
*/
/* feedback elements necessary to realize this as an active inductor
*/
/* using the topology shown in Campbell's thesis.
*/
#include <stdio.h>
#include <float.h>
#include <math.h>

main()
{
```

```

double gm1, gm2, rpi1, rpi2, cpi1, cpi2, l_in, r_in, lim1, lim2, sugg_r;
double pole1, pole2, k, sigma_z, a, b, rf1, rf2, cf1, cf2;
double min_r, max_r;
char temp[40], ans;

puts( "Type in value of gm1" );
scanf( "%40s", temp );
gm1 = atof( temp );

puts( "Type in value of gm2" );
scanf( "%40s", temp );
gm2 = atof( temp );

puts( "Type in value of Rpi1" );
scanf( "%40s", temp );
rpi1 = atof( temp );

puts( "Type in value of Rpi2" );
scanf( "%40s", temp );
rpi2 = atof( temp );

puts( "Type in value of Cpi1" );
scanf( "%40s", temp );
cpi1 = atof( temp );

puts( "Type in value of Cpi2" );
scanf( "%40s", temp );
cpi2 = atof( temp );

do
{
    puts( "Type in desired value of Lin" );
    scanf( "%40s", temp );
    l_in = atof( temp );

    pole1 = 1 / ( rpi1 * cpi1 );
    pole2 = 1 / ( rpi2 * cpi2 );
    lim1 = l_in * pole1 + 1/ gm2;
    lim2 = l_in * pole2 + (1/gm2)*gm1/(gm1 + 1/rpi1 - cpi1/(rpi2*cpi2));
    sugg_r = sqrt( lim1 * lim2 );
    if( lim1 > lim2 )
    {
        min_r = lim2;
        max_r = lim1;
    }
    else
    {
        min_r = lim1;
        max_r = lim2;
    }

    printf( "Rin must lie between %1.4e and %1.4e ohms, suggest %1.4e\n",
min_r, max_r, sugg_r );
    puts( "Type in desired value of Rin" );
    scanf( "%40s", temp );
    r_in = atof( temp );

    printf( "\ngm1 = %1.4e    gm2 = %1.4e\n", gm1, gm2 );
    printf( "Rpi1 = %1.4e    Rpi2 = %1.4e\n", rpi1, rpi2 );
    printf( "Cpi1 = %1.4e    Cpi2 = %1.4e\n", cpi1, cpi2 );
}

```

```

printf( "Lin = %1.4e    Rin = %1.4e\n", l_in, r_in );

k = gm2 *( l_in*gm1 + cpi1*r_in - l_in*cpi1*pole2 ) / (cpi1*cpi2);
sigma_z = r_in*(gm1 + 1/rpi1) - (l_in*pole2)/rpi1 - gm1/gm2;
sigma_z = sigma_z / ( l_in*( gm1 - cpi1*pole2 ) + r_in*cpi1 );
a = k*( sigma_z - pole1 )/( pole2 - pole1 );
b = k*( sigma_z - pole2 )/( pole1 - pole2 );

rf1 = rpi1*cpi1*a;
cf1 = 1/a;
rf2 = rpi2*cpi2*b;
cf2 = 1/b;

/* printf( "K = %1.4e  Sigma_z = %1.4e\n", k, sigma_z );
   printf( "A = %1.4e  B = %1.4e\n", a, b );
*/
if ( !( ( (pole1>sigma_z)&&(sigma_z>pole2) ) || (
(pole2>sigma_z)&&(sigma_z>pole1) ) ) ) )
{
    printf( "Not physically realizable, zero is not between
poles\n" );
    printf( "Pole1 = %1.4e    Zero = %1.4e    Pole2 = %1.4e\n",
pole1, sigma_z, pole2 );
}
printf( "\nRf1 = %1.4e    Cf1 = %1.4e\n", rf1, cf1 );
printf( "Rf2 = %1.4e    Cf2 = %1.4e\n\n", rf2, cf2 );
puts( "Want to try another value of Lin and Rin ?" );
ans = getch();
} while( ans != 'N' && ans != 'n' );
}

```

APPENDIX B: NE681 MODEL PARAMETERS

```

* FILENAME           : NE68100.MDL
* NEC PART NUMBER:  NE68100
* CEL DERIVED       : MAY 1991
* BIAS CONDITIONS:  VCE=8V, IC=7mA and VCE=8V, IC=20mA
* FREQ RANGE FOR SIMULATION VERIFICATION: 1.5GHZ TO 10GHZ
* BASE: TOTAL 1 WIRE, 1 PER BOND PAD, 0.0134" (340um)
*   LONG EACH WIRE
* COLLECTOR:TOTAL 1 WIRE, 1 PER BOND PAD, 0.0083" (210um)
*   LONG EACH WIRE
* EMITTER:  TOTAL 2 WIRES, 2 PER SIDE, 0.0176" (446um)
*   LONG EACH WIRE
* WIRE: 0.0007" (17.8um) DIAMETER GOLD
* BOND WIRE INDUCTANCES USED FOR SIMULATION ARE:
*   Lb=.18E-9  Lc=.01e-9  Le=.15E-9
* CHIP CAPACITANCES USED FOR SIMULATION ARE:
*   C(base to collector)=.07pF  C(collector to emitter)=.01pF

```

.MODEL NE681 NPN

```

+ IS=2.7E-16      BF=185          NF=1.02  VAF=15    IKF=0.055
+ ISE=1.77E-11   NE=2.1  BR=1    VAR=0    IKR=0
+ RB=12  RE=.6   RC=8   CJE=1.2E-12  VJE=.77  MJE=.5
+ TF=1.4E-11     CJC=.8E-12  VJC=.27  MJC=.56  XCJC=0
+ ITF=.1  IRB=12e-6  NR=1  RBM=3.7  TR=.3e-9
+ VTF=25  XTF=3

```


APPENDIX C: NETLIST FOR CASE 1

```

* ACTIVE INDUCTOR, CASE 1 BIAS
*
.INCLUDE NE68100.MDL
.PARAM DRV = .02
.AC DEC 40 1MEG 10G
.STEP PARAM DRV LIST .0001 .0002 .0005 .001 .002 .005 .01
*
* Include for 100 MHz analysis.
*.TRAN 0.02442002NSEC 300NSEC 200NSEC 0.02442002NSEC
*.FOUR 100MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 100MEG 0 0 0) AC 1
*
* Include for 200 MHz analysis.
*.TRAN 0.012210012NSEC 250NSEC 200NSEC 0.012210012NSEC
*.FOUR 200MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 200MEG 0 0 0) AC 1
*
* Include for 500 MHz analysis.
*.TRAN 4.8840048PSEC 220NSEC 200NSEC 4.8840048PSEC
*.FOUR 500MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 500MEG 0 0 0) AC 1
*
* Include for 1000 MHz analysis.
*.TRAN 0.002442002NSEC 210NSEC 200NSEC 0.002442002NSEC
*.FOUR 1000MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 1000MEG 0 0 0) AC 1
.OP
.OPTIONS ITL5=0
.PROBE V([IN]) I(C_IN)
R_IN 0 INPUT 1MEG
C_IN INPUT IN 1U
L_CCE 6 9 1U
L_CCB 4 10 1U
C_COUP 5 6 1U
C_BLK 4 3 1U
L_CEB 5 8 1U
L_CEC IN 7 1U
R_CEB 11 8 88.1K
R_CCB 12 10 99K
R_FB2 2 3 9621
C_FB2 2 3 0.296PF
R_FB1 IN 2 10767
C_FB1 IN 2 0.373PF
V_CCB 12 9 DC 5.1V
V_CE 7 0 DC 8V
V_CC 0 9 DC 8V

```

V_CEB 11 0 DC 9.8V
Q1 0 4 6 NE681
Q2 IN 5 0 NE681
.END

APPENDIX D: NETLIST FOR CASE 2

```

* ACTIVE INDUCTOR, CASE 2 BIAS
*
.INCLUDE NE68100.MDL
.PARAM DRV = .02
.AC DEC 40 1MEG 10G
.STEP PARAM DRV LIST .0001 .0002 .0005 .001 .002 .005 .01
+.05
*
* Include for 100 MHz analysis.
*.TRAN 0.02442002NSEC 300NSEC 200NSEC 0.02442002NSEC
*.FOUR 100MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 100MEG 0 0 0) AC 1
*
* Include for 200 MHz analysis.
*.TRAN 0.012210012NSEC 250NSEC 200NSEC 0.012210012NSEC
*.FOUR 200MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 200MEG 0 0 0) AC 1
*
* Include for 500 MHz analysis.
*.TRAN 4.8840048PSEC 220NSEC 200NSEC 4.8840048PSEC
*.FOUR 500MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 500MEG 0 0 0) AC 1
*
* Include for 1000 MHz analysis.
*.TRAN 0.002442002NSEC 210NSEC 200NSEC 0.002442002NSEC
*.FOUR 1000MEG V([IN]) I(C_IN)
*I_IN 0 INPUT SIN(0 {DRV} 1000MEG 0 0 0) AC 1
.OP
.OPTIONS ITL5=0
.PROBE V([IN]) I(C_IN)
R_IN 0 INPUT 1MEG
C_IN INPUT IN 1U
L_CCE 6 9 1U
L_CCB 4 10 1U
C_COUP 5 6 1U
C_BLK 4 3 1U
L_CEB 5 8 1U
L_CEC IN 7 1U
R_CEB 11 8 19.18K
R_CCB 12 10 99K
R_FB2 2 3 6891
C_FB2 2 3 0.392PF
R_FB1 IN 2 8471
C_FB1 IN 2 0.474PF
V_CCB 12 9 DC 5.1V
V_CE 7 0 DC 8V

```

```
V_CC 0 9 DC 8V
V_CEB 11 0 DC 9.8V
Q1 0 4 6 NE681
Q2 IN 5 0 NE681
.END
```